学习

system-verilog

#system-
verilog

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1: system-verilog

SystemVerilog[Verilog]。 AccelleraVerilog [IEEE Std 1364-2001](SystemVerilog2005IEEE。 2009 IEEEVerilogIEEE 1364SystemVerilogIEEE 1800。 SystemVerilogFPGAASIC。 SystemVerilog HDL。

SystemVerilog3

- RTL。

- 。 [OVM VMM UVM]

- 。

SystemVerilog [IEEE Std 1800-2012]	2013221
SystemVerilog [IEEE Std 1800-2009]	2009-12-11
SystemVerilog [IEEE Std 1800-2005]	2005-11-22

Examples

SystemVerilog。 EDA

- Cadence Incisive
- Mentor Graphics QuestaSim
- Synopsys VCS

EDA

- Aldec Riviera-PRO
- Xilinx Vivado

LRM

- Verilator

```
// File 'test.sv'

// Top module that gets instantiated automatically when simulation is started
module test;

  // Thread gets started at the beginning of the simulation
  initial begin

    // Call to system task to print output in simulator console
    $display("Hello world!");
```

```
    end

endmodule
```

Cadence Incrisive

```
irun test.sv
```

system-verilog https://riptutorial.com/zh-CN/system-verilog/topic/2829/system-verilog

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